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HIGH-PERFORMANCE 32-BIT BCD ADDER ARCHITECTURE FOR ADCA DEFENSE SYSTEMS

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Abstract--- In today's technology environment, systems must be compact, light, and fast with minimal latency while handling data. When building these circuits, we need a new approach to satisfy these expectations. This article introduces a novel design approach called Quantum-dot Cellular Automata (QCA). Using QCA, we can make great strides in designing more complicated circuits. In this study, we provide a new approach to building QCA-based 32-bit BCD adders. Decimal arithmetic, majority gates (MG), low power, binary coded-decimal adders, and quantum-dot cellular automata (QCA) are some of the topics discussed.

INTRODUCITON

The basic limit will be approached by CMOS with continued and rapid dimensional scaling. Additionally, existing CMOS technology devices are limited in their ability to scale further due to short channel effects, high power dissipation, and quantum effects [2-3]. New device technologies are able to circumvent the scaling constraint of CMOS technology. Some of the technologies that fall within the category of "Beyond CMOS" are SETs, QCAs, and RTDs, or resonant tunnelling diodes. We recommend Quantum-dot Cellular Automata over all of these developing nanotechnologies. You can get a device density of 1012 devices/cm2 and an operating speed of THz using QCA, a transistor-less computing paradigm. By using the quantum effects of tiny scale, the QCA device paradigm supplants logic based on field effect transistors. A quantum-dot cellular automaton is a way to achieve device performance via the coupling of cells that represent binary information but do not conduct current.

This Paper is Organized as follows Section II will gives you the details of the software used to prepare this project, Section III deals with the Structure of QCA cell and its polarization and QCA background Section IV gives you the design and implementation efficient 32-bit BCD adder, Section V deals with the outcome of the project and finally Section VI gives the Conclusion and Future Scope & some of the references of this project.

I. SOFTWAREUSED

QCA designer is the product of an ongoing effect to create a rapid and accurate simulation and layout tool. for quantum-dot cellular automata (QCA). It is capable of simulating complex QCA circuits on most standard platforms. And it is an ongoing research effect by the Walus Lab at the University of British Coloumbia to create a design and simulation tool for QCA. This tool is still under development and is provided free of cost to the research community "as is". QCA is an emerging concept in computational nanotechnology for the realization of computer using arrays of nano-scale QCA cells. These QCA cells are capable of performing all complex computational functions required for general- purpose computation (majority function, Inversion, and fan-out). The QCADesigner tool facilitates rapid design, layout and simulation of QCA circuits by providing powerful CAD features available in more complex circuit design tools.

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II. STRUCTURE OF QCA CELL ANDPOLARIZATION

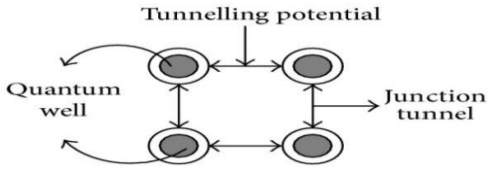


Fig. 1 Structure of a QCA Cell

The most fundamental element of the QCA structure is shown in figure 1. It is the building block of the QCA technology. As

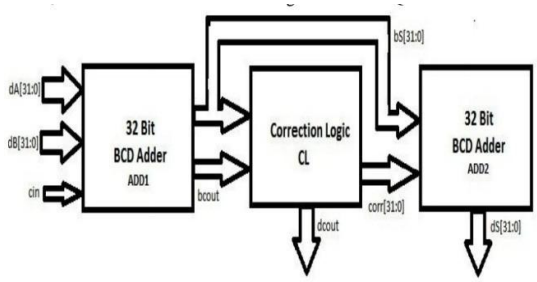
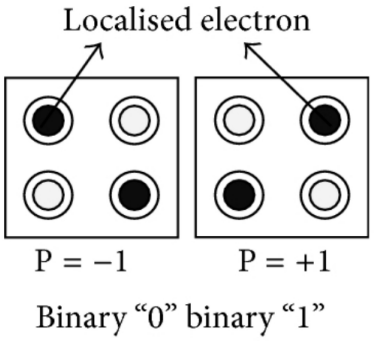


Fig 3.Structure of the 32 bits BCD adder.

we can see in the figure it is having four dots at all its corner. The structure has two free electrons. The structure of the QCA in provided in
the figure 1.



Because of the coulombic repulsion these two electrons can only be placed in two stable states. The electrons are always resided in diagonally opposite corners of the QCA cell. The diagonally opposite corners are having maximum distance. The stable states also called as polarization. As per the locations of the electrons in the cell two states can be take place. These states are considered as binary states 1 and 0. For the purpose of explanation the figure 2 is shown.

The diagonally opposite electrons interact to each other by the electrostatic forces and due to this force the electrons maintain its polarization. However the QCA cells cannot flow the data intrinsically therefore to get the control over flow of the direction of electrons the four clock zones are associated. These four clock signal have 90◦ phase difference. The QCA design is partitioned into clock zones. The clock scheme, named the zone clocking scheme, makes the QCA designs different polarizations intrinsically
pipelined.

32 BIT BCD ADDER

In brief this proposes a unique approach to develop a QCA- based 32 bits BCD adder which can achieve higher computational speed than existing counterparts with occupying less area or count cell. The novel 1-digit decimal adder generates, propagates, and absorbs a carry signal with delay times up to 27%, 45%, and 44% lower than the faster existing counterparts that are those described in differently from all previous works, we extended our work to the design of a 32-bits QCA- based BCD adder.

The BCD adder here presented follows the traditional top-level structure illustrated in Fig. 3, but it

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exploits the novel logic expressions demonstrated in the following by Equations1 and 2.

As the main result, the proposed approach leads to the best trade off between the overall occupied area and thespeed performances.
To understand the new design strategy, let us examine first the 4 bits binary adder ADD1. 4 bit binary adder ADD1 collects the value of input dA(3:0) and dB(3:0) as well as its carry “cin” and figure

out its binary output as bS(3:0) and “bcout”, this whole process it carried out as per the equation (2a) that introduces only one Majority gate(MG) between Ci and Ci+1.

Generally BCD means Binary Coded Decimal as we know decimal values means 0-9 so that if the output of the BCD adder result is greater than 9 or when the carry is "1" then we Add 6 to the obtained output to get the valid BCD Value. The reason for to add 6 to the UNBCD output is the in hexadecimal the difference between the maximum value and to the 9 is 6.
And this 32 bit BCD adder consists of 2 32bit binary adders and correction logic which consists of AND & OR gates .

III. OUTPUT

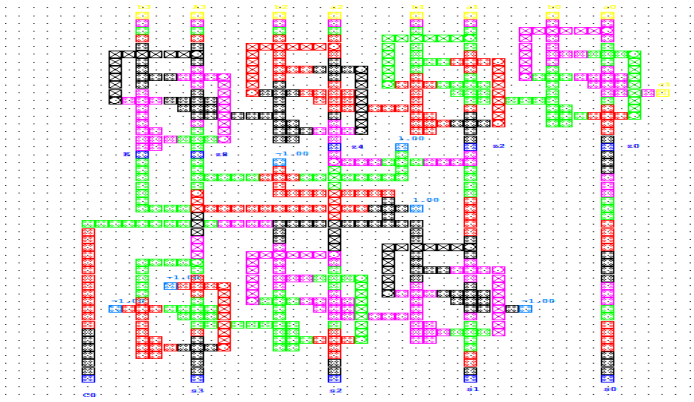

Fig 1 digit BCD adder in QCA.

So here the QCA implementation shows that we need4 full adder at thetop of the block for adding two 4bit binary numbers and there is a correction logic which consists of AND& OR gates.

And we need 3 Full Adders at the bottom to add 6 0r 0 to the output of the first 4 full adders.

Generally we developed 1 digit BCD adder in QCA due to circuit complexity and increase in th.

SIMULATION WAVEFORM

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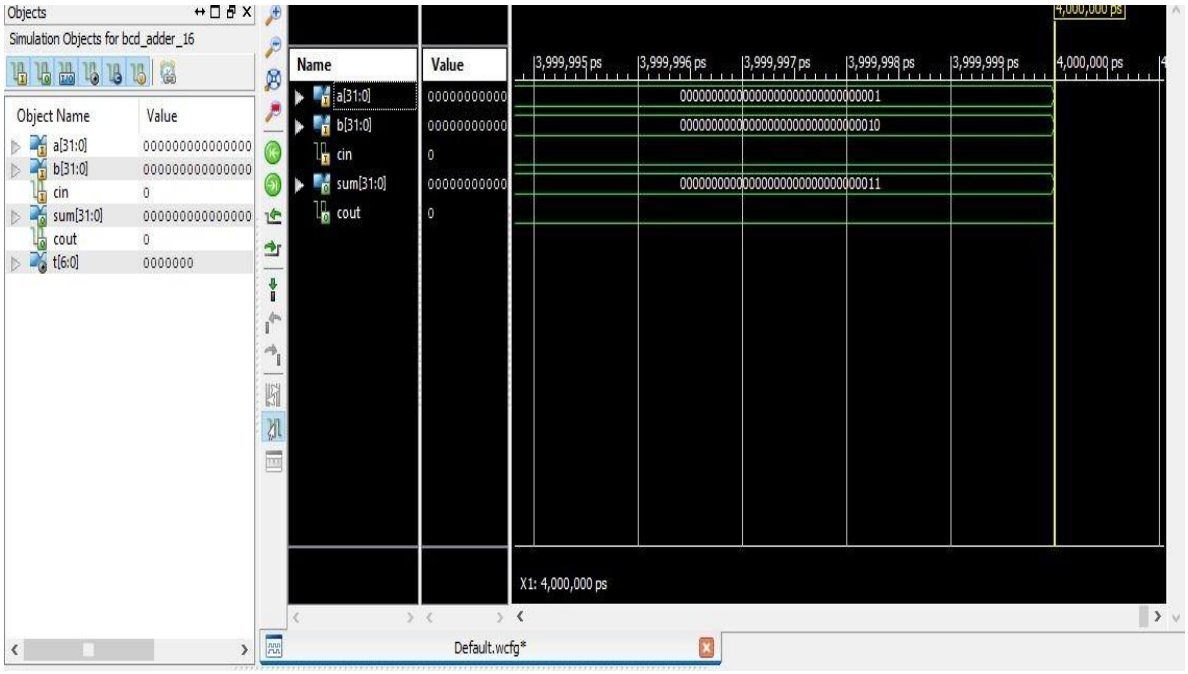
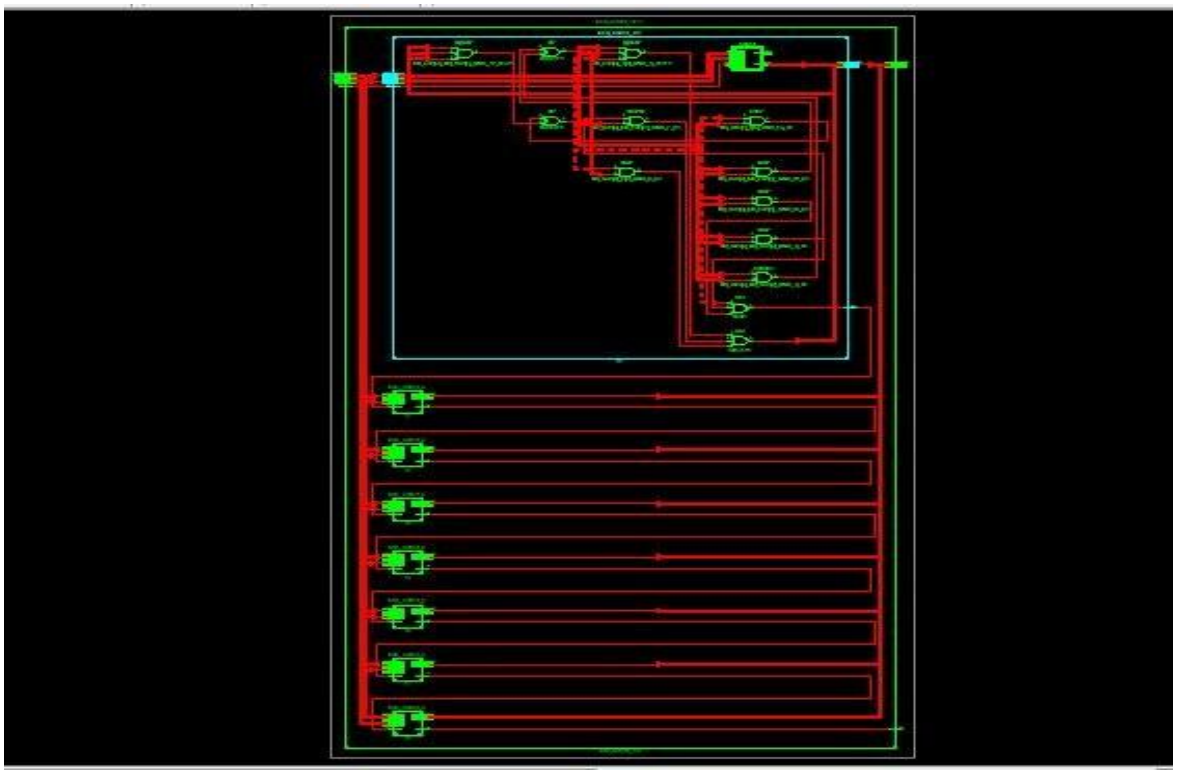


RTL SCHEMATIC



The figure shows the RTL schematic of the 32 bit BCD adder In this we have first developed an VHDL code for

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the 4 bit BCD adder then with the help of this 4 bit BCD adder we have developed 32 bit BCD adder

Here we have used Eight 4 bit BCD adders the output of one 1 digit BCD adder is added as the Carryin to next 1 digit BCD adder and at last the output of the 8th BCD adder is taken as cout.

VI . CONCLUSION

In order to create a 32-bit BCD adder, the proposed work primarily focuses on combining two 32-bit BCD adders using binary adders. If the result is not a valid BCD value, an additional 6 is added to the total. This allowed us to create the BCD adder's simulation waveforms and RTL schematic.

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